CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A charge pump circuit for generating a pumped voltage, comprising:

first charge pump means responsive to a first set of clock signals;

second charge pump means responsive to a second set of clock signals different from the first clock signals; ~~and~~

means for selectively connecting the second charge pump means in series with the first charge pump means in response to a mode signal; and

means for selectively bypassing the second charge pump means to generate the pumped voltage in response to the mode signal.

2. (Currently Amended) The charge pump circuit of Claim 1, wherein the first charge pump means includes threshold voltage cancellation circuitry.

3. (Currently Amended) The charge pump circuit of Claim 2, wherein the second charge pump means does not include threshold voltage cancellation circuitry.

4. (Currently Amended) The charge pump circuit of Claim 1, wherein ~~the means for selectively connecting comprises~~:

the means for selectively bypassing comprises a first switch responsive to the mode signal and coupled between an output node of the first charge pump means and a voltage rail; and

the means for selectively connecting comprises a second switch responsive to the mode signal and coupled between the output node of the first charge pump means and an input node of the second charge pump means.

5. (Currently Amended) The charge pump circuit of Claim 4, wherein the first switch comprises:

one or more transistors connected in series between the voltage rail and the output node of the first charge pump means; and

a level shifter circuit having an input responsive to the mode signal and having an output connected to the gates of at least one of the one or more transistors.

6. (Currently Amended) The charge pump circuit of Claim 4, wherein the second switch comprises:

a pass transistor connected in series between the output node of the first charge pump means and the input node of the second charge pump means; and

a level shifter circuit having an input responsive to the mode signal and having an output connected to the gate of the pass transistor.

7. (Currently Amended) The charge pump circuit of Claim 1, wherein the first set of clock signals comprises a four-phase oscillation signal and the second set of clock signals comprises a two-phase oscillation signal.

8. (Currently Amended) The charge pump circuit of Claim 7, wherein the first set of clock signals has a voltage swing approximately equal to a supply voltage (VCC) and the second set of clock signals has a boosted voltage swing approximately equal to 2*VCC.

9. (Currently Amended) The charge pump circuit of Claim 8, wherein the second set of clock signals has a logic high voltage level approximately equal to VCC and has a logic low voltage level approximately equal to –VCC.

10. (Canceled)

11. (Currently Amended) A charge pump circuit for generating a pumped voltage on a voltage rail, comprising:

a first charge pump including a plurality of first charge pump stages responsive to a four-phase oscillation signal;

a second charge pump including a plurality of second charge pump stages responsive to a two-phase ~~clock~~ oscillation signal; and

a switching circuit having a first terminal connected to an output of the first charge pump, a second terminal connected to an input of the second charge pump, a third terminal connected to the voltage rail, and a control terminal to receive a mode signal.

12. (Currently Amended) The charge pump circuit of Claim 11, wherein the switching circuit selectively connects ~~only~~ the first charge pump to the voltage rail when the mode signal is in a first state.

13. (Currently Amended) The charge pump circuit of Claim 12, wherein the switching circuit connects the first and second charge pumps together in series with the voltage rail when the mode signal is in a second state.

14. (Canceled)

15. (Currently Amended) The charge pump circuit of Claim 14, wherein one or more of the first charge pump stages includes threshold voltage cancellation circuitry, and the second charge pump stages do not include threshold voltage cancellation circuitry.

16. (Currently Amended) The charge pump circuit of Claim 11, wherein the four-phase oscillation signal has a voltage swing approximately equal to a supply voltage (VCC) and the two-phase oscillation signal has a voltage swing approximately equal to 2*VCC.

17. (Currently Amended) The charge pump circuit of Claim 16, wherein the two-phase oscillation signal has a logic high voltage level approximately equal to VCC and has a logic low voltage level approximately equal to –VCC.

18. (Currently Amended) The charge pump circuit of Claim 11, wherein the pumped voltage is a negative pumped voltage, and the voltage rail is a negative voltage rail.

19. (Original) A charge pump circuit, comprising:

a plurality of charge pumps, each selectively connected in parallel with each other in response to a corresponding select signal to generate various drive currents for a pumped voltage on a voltage rail, and each comprising:

first charge pump means responsive to a first set of clock signals;

second charge pump means responsive to a second set of clock signals different from the first clock signals; and

means for selectively connecting the second charge pump means in series with the first charge pump means in response to a mode signal.

20. (Currently Amended) The charge pump circuit of Claim 19, wherein each of the means for selectively connecting comprises a first terminal connected to an output of the corresponding first charge pump means, a second terminal connected to an input of the corresponding second charge pump means, a third terminal connected to the voltage rail, and a control terminal to receive the mode signal.

21. (Currently Amended) The charge pump circuit of Claim 19, wherein each of the means for selectively connecting comprises:

a first switch responsive to the mode signal and coupled between an output node of the corresponding first charge pump means and the voltage rail; and

a second switch responsive to the mode signal and coupled between the output node of the corresponding first charge pump means and an input node of the corresponding second charge pump means.

22. (Currently Amended) The charge pump circuit of Claim 21, wherein each of the first ~~switch~~ switches comprises:

one or more transistors connected in series between the voltage rail and the output node of the corresponding first charge pump means; and

a level shifter circuit having an input responsive to the mode signal and having an output connected to the gates of at least one of the one or more transistors.

23. (Currently Amended) The charge pump circuit of Claim 21, wherein each of the second ~~switch~~ switches comprises:

a pass transistor connected in series between the output node of the corresponding first charge pump means and the input node of the corresponding second charge pump means; and

a level shifter circuit having an input responsive to the mode signal and having an output connected to the gate of the pass transistor.

24. (Canceled)

25. (Currently Amended) The charge pump circuit of Claim 19, wherein each of the first charge pump means includes threshold voltage cancellation circuitry, and each of the second charge pump means does not include threshold voltage cancellation circuitry.

26. (Currently Amended) The charge pump circuit of Claim 19, wherein the first set of clock signals comprises a four-phase oscillation signal and the second set of clock signals comprises a two-phase boosted oscillation signal.

27. (Currently Amended) The charge pump circuit of Claim 26, wherein the first set of clock signals has a voltage swing approximately equal to a supply voltage (VCC) and the second set of clock signals has a voltage swing approximately equal to 2*VCC.

28. (Currently Amended) The charge pump circuit of Claim 27, wherein the second set of clock signals has a logic high voltage level approximately equal to VCC and has a logic low voltage level approximately equal to –VCC.

29. (Currently Amended) The charge pump circuit of Claim 19, further comprising:

a plurality of switching circuits, each having an input connected to an output of a corresponding one of the plurality of charge pumps, an output connected to the voltage rail, and a control terminal to receive a corresponding select signal.

30. (Currently Amended) The charge pump circuit of Claim 29, wherein each of the switching circuits ~~comprise PMOS transistors~~ comprises a PMOS transistor.

31. (Currently Amended) The charge pump circuit of Claim 19, wherein each of the plurality of charge pumps further comprises:

a first logic gate configured to selectively disable the first set of clock signals in response to a corresponding select signal; and

a second logic gate configured to selectively disable the second set of clock signals in response to the corresponding select signal.

32. (Currently Amended) The charge pump circuit of Claim 31, wherein the each of first and second logic gates ~~comprise AND gates~~ comprises an AND gate.

33. (Currently Amended) The charge pump circuit of Claim 19, wherein the plurality of charge pumps is a plurality of negative charge pumps, the pumped voltage is a negative pumped voltage, and the voltage rail is a negative voltage rail.

34. (Currently Amended) A charge pump circuit for generating various pumped voltages on a voltage rail with various drive currents, comprising:

a plurality of charge pumps, each including an output terminal and comprising:

a first charge pump including a plurality of first charge pump stages ~~configured to generate pumped voltages in an optimally efficient manner~~;

a second charge pump including a plurality of second charge pump stages ~~configured to generate a maximum pumped voltage~~; and

a first switching circuit configured to selectively connect the second charge pump in series with the first charge pump in response to a mode signal; and

a plurality of second switching circuits, each having an input coupled to the output terminal of a corresponding charge pump, an output coupled to the voltage rail, and a control terminal to receive a corresponding select signal.

35. (Currently Amended) The charge pump circuit of Claim 34, wherein each of the first switching ~~circuit~~ circuits comprises a first terminal connected to an output of the corresponding first charge pump, a second terminal connected to an input of the corresponding second charge pump, a third terminal connected to the voltage rail, and a control terminal to receive the mode signal.

36. (Currently Amended) The charge pump circuit of Claim 35, wherein each of the first switching ~~circuit~~ circuits comprises:

a first switch responsive to the mode signal and coupled between the output ~~node~~ of the corresponding first charge pump and the voltage rail; and

a second switch responsive to the mode signal and coupled between ~~an~~ the output ~~node~~ of the corresponding first charge pump and an input ~~node~~ of the corresponding second charge pump.

37. (Currently Amended) The charge pump circuit of Claim 34, wherein each of the first charge pumps ~~are~~ is controlled by a four-phase oscillation signal and each of the second charge pumps ~~are~~ is controlled by a two-phase oscillation signal.

38. (Currently Amended) The charge pump circuit of Claim 37, wherein the four-phase oscillation signal has a voltage swing approximately equal to a supply voltage (VCC) and the two-phase oscillation signal has a voltage swing approximately equal to 2*VCC.

39. (Currently Amended) The charge pump circuit of Claim 38, wherein the two-phase oscillation signal has a logic high voltage level approximately equal to VCC and has a logic low voltage level approximately equal to –VCC.

40. (Currently Amended) The charge pump circuit of Claim 34, wherein each of the first charge pumps ~~include~~ includes threshold voltage cancellation circuitry and each of the second charge pumps ~~do~~ does not include threshold voltage cancellation circuitry.

41. (Currently Amended) The charge pump circuit of Claim 34, wherein the pumped voltages are negative pumped voltages, the voltage rail is a negative voltage rail, and the plurality of charge pumps is a plurality of negative charge pumps~~, the plurality of first charge pump stages is configured to generate negative pumped voltages in an optimally efficient manner, and the plurality of second charge pump stages is configured to generate a maximum negative pumped voltage~~.

42. (Currently Amended) A method for generating pumped voltages on a voltage rail, comprising:

selectively connecting a plurality of charge pump circuits in parallel with each other in response to a plurality of corresponding select signals to adjust the drive current on the voltage rail; and

within each of the charge pump circuits, selectively connecting a second charge pump circuit in series with a first charge pump circuit in response to a mode signal to adjust the magnitude of the pumped ~~voltage~~ voltages generated on the voltage rail.

43. (Original) The method of Claim 42, wherein asserting the mode signal connects the first and second charge pumps in series between input and output terminals of the corresponding charge pump circuit.

44. (Original) The method of Claim 42, wherein de-asserting the mode signal connects only the first charge pump between input and output terminals of the corresponding charge pump circuit.

45. (Original) The method of Claim 42, wherein asserting the select signal connects the output terminal of the corresponding charge pump circuit to the voltage rail.

46. (Original) The method of Claim 42, wherein de-asserting the select signal disconnects the output terminal of the corresponding charge pump circuit from the voltage rail.

47. (Original) The method of Claim 42, wherein de-asserting the select signal disables the corresponding charge pump circuit by forcing its input clock signals to logic low.

48. (Original) The method of Claim 42, wherein the pumped voltages are negative pumped voltages, the voltage rail is a negative voltage rail, and the plurality of charge pump circuits is a plurality of negative charge pump circuits.